Yulong Tang

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Education

Renmin University of China — Beijing, China
M.S. in Software Engineering — 2024 - 2026
Research area: Computer Systems
GPA: 3.42/4.00

University of Electronic Science and Technology of China — Chengdu, China
B.E. in Network Engineering — 2019 - 2023
GPA: 3.56/4.00

Publications

[1] Zhongjie Chen, Wentao Zhang, **Yulong Tang**, Ran Shu, Fengyuan Ren, Tianyin Xu, Jing Liu. *Principled Performance Tunability in Operating System Kernels.* Under submission to OSDI'26.

Research Experience

Microsoft Research Asia | Research Intern, Mentor: Jing Liu — 2025.07 – Now

- Designed experiments and custom workloads to explore the impact of kernel constants on system performance. Demonstrated clear performance gains from runtime tuning by identifying scenarios where default values are suboptimal.
- Collected a dataset of kernel constants and implemented approximately 80 test cases to evaluate the mechanism's correctness and robustness. The testing framework focused on:
  - Stable triggering of target kernel code paths.
  - Internal measurement and verification of the tuning logic.
  - Reproducibility of results across repeated experimental runs.

Inria KrakOS Lab | Remote RA, Supervisor: Baptiste Lepers — 2025.03 – 2025.08

- *DSwap* is an adaptive swapping algorithm that distributes paging traffic between compressed in-memory swapping and SSD-based swapping. Because the relative benefit of compressed versus SSD swapping depends on data compressibility, CPU load, and I/O load, choosing an effective distribution strategy is non-trivial.
- Conducted about 2,000 core-hours of experiments on the Grid'5000 cluster and analyzed and visualized the results to characterize *DSwap*'s performance under different machine configurations. These experiments revealed that *DSwap* is not always optimal on nodes with heterogeneous SATA+SSD storage and suggested that strong read/write speed asymmetry may limit its effectiveness.

Beijing Institute of Open Source Chip | Technical Development Intern 2024.06 – 2024.08

- Implemented a simplified QEMU-like full-system emulator (NEMU) for RISCV32 architecture. Key contributions include:
  - Built-in Debugger (sdb): Supported single-step execution, register/memory inspection, and watchpoint management (suspending execution on variable changes).
  - Efficient Simulation: Utilized C macros to template RISC-V instructions, improving scalability and error detection; supported standard library functions (sprintf, memset, etc.).
  - I/O Support: Implemented basic devices (serial, timer, keyboard, VGA). Successfully ran classic games like Super Mario via FCEUX emulator.
  - OS & FS Support: Implemented exception handling for system calls (Nanos-lite) and built a simple file system supporting ramdisk I/O.

Honors and Awards

Outstanding Student Scholarship UESTC, 2020

Service

Artifact Evaluation Committee: SOSP'25, EuroSys'26